CLAIMS

We claim:

1. A frame reconstruction circuit for reconstructing a block of video data that has been subject to MPEG compression, the block of video data including a plurality of pixels arranged in a horizontal and vertical array, and comprising:

a first interpolation element having an input terminal for receiving data representing the pixels of the block of video data, wherein the first interpolation element averages data representing a first pixel of the block of data with data representing a second pixel adjacent in a first direction in the block of data to the first pixel, and providing the averaged value at an output terminal;

a second interpolation element having an input terminal coupled to the output terminal of the first interpolation element, wherein the second interpolation element averages an averaged value from the first interpolation element with an averaged value from the first interpolation element associated with a set of pixels of the block of data adjacent in a second direction orthogonal to the first direction, the second interpolation element having an output terminal for providing the average of the two averaged values at the output terminal; and

a selector element having an input terminal coupled to the output terminal of the second interpolation element, wherein the selector element selectably provides at its output terminal a value representing one of:

a) an externally provided signal;

b) the average of the two averaged values from the second interpolation element;

c) a sum of the externally provided signal and the average of the two averaged values.

2. The circuit of Claim 1, further comprising a first storage element coupled between the output terminal of the first interpolation element and the input terminal of the second interpolation element, and a second storage element coupled between the output terminal of the second interpolation element and the input terminal of the selector element.

3. The circuit of Claim 1, wherein the first interpolation element includes:

a flip-flop having an input terminal and an output terminal, the flip-flop input terminal being coupled to the input terminal of the first interpolation element;

a multiplexer having a control terminal, first and second input terminals, and an output terminal, the input terminals of the multiplexer being coupled respectively to the input terminal of the first interpolation element and to the output terminal of the flip-flop; and

an adder having two input terminals coupled respectively to the output terminal of the multiplexer and the output terminal of the flip-flop, and having an output terminal coupled to the output terminal of the first interpolation element.

4. The circuit of Claim 1, wherein the second interpolation element includes:

a shift register having an input terminal coupled to the input terminal of the second interpolation element and having an output

terminal;

a multiplexer having two input terminals coupled respectively to the output terminal of the shift register and the input terminal of the second interpolation element, a control terminal, and an output terminal; and

an adder having two input terminals coupled respectively to the output terminal of the shift register and to the output terminal of the multiplexer, and having an output terminal coupled to the output terminal of the second interpolation element.

5. The circuit of Claim 4, wherein the shift register includes:

an n stage shift register element, where $n \geq 8$;

a one-stage shift register element; and

a multiplexer having two input terminals connected respectively to an output terminal of the n stage shift register element and to an output terminal of the one-stage shift register element.

6. The circuit of Claim 1, wherein the selector element includes:

a first multiplexer having two input terminals connected respectively to the output terminal of the second interpolation element and to a reference value;, and having an output terminal and a control terminal;

a second multiplexer having two input terminals connected respectively to receive the externally provided signal and a reference value, and having an output terminal and a control terminal; and

an adder having two input terminals coupled respectively to the output terminals of the first and second multiplexers, and having an output terminal coupled to the output terminal of the selector element.

7. The circuit of Claim 1, wherein the input terminal of the first interpolation element and the output terminal of the selector element are each 8-bit parallel data ports, and the circuit has at least an internal bus structure of at least 8 bits.

8. The circuit of Claim 1, further comprising a second data path for bidirectional processing, comprising:

an additional first interpolation element; and

an additional second interpolation element;

wherein each of the additional interpolation elements are serially coupled in parallel to the first and second interpolation elements.

9. The circuit of Claim 1, further comprising a feedback path coupling the output terminal of the selector element to the input terminal of the first interpolation element.

10. The circuit of Claim 1, wherein one of the first and second interpolation elements is a horizontal interpolation element, another being a vertical interpolation element.

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11. A method of reconstructing a block of video data that has been subject to MPEG compression, the block including a plurality of pixels arranged horizontally and vertically in an array, the method

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comprising:

first, selectively averaging values associated with two pixels adjacent in a first direction in the block;

second, selectively averaging two of the selectively averaged values associated with two sets of pixels adjacent in a second direction orthogonal in the first direction; and

selectively providing as an output signal one of:

a) an externally provided signal;

b) a result of the second step of selectively averaging;

c) a sum of the externally provided signal and the result of the second step of selectively averaging.

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